

**INTEGRATED CIRCUIT SUBSTRATE HAVING EMBEDDED LANDS WITH ETCHING
AND PLATING CONTROL SHAPES**

Ronald Patrick Huemoeller
David Jon Hiner
Sukianto Rusli
Richard Sheridan

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation-in-part of the following co-pending U.S. Patent applications: "IMPRINTED INTEGRATED CIRCUIT SUBSTRATE AND METHOD FOR IMPRINTING AN INTEGRATED CIRCUIT SUBSTRATE" Serial number 09/931,144 filed August 16th, 2001; "INTEGRATED CIRCUIT SUBSTRATE HAVING LASER-EMBEDDED CONDUCTIVE PATTERNS AND METHOD THEREFOR", serial number 10/138,225 filed May 1, 2002; "SOLDERABLE INJECTION-MOLDED INTEGRATED CIRCUIT SUBSTRATE AND METHOD THEREFOR" serial number 09/931,144, filed August 16, 2001; and "INTEGRATED CIRCUIT FILM SUBSTRATE HAVING EMBEDDED CONDUCTIVE PATTERNS AND VIAS", serial number 10/261,868 filed October 1, 2002. Each of the above-listed parent applications has at least one common inventor and is assigned to the same assignee. The specifications of all of the above-listed parent applications are incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates generally to semiconductor packaging, and more specifically, to a substrate having embedded

conductors and lands for providing an electrical interface between a die and external terminals in an integrated circuit package, wherein etching and plating control shapes are incorporated in the lands.

BACKGROUND OF THE INVENTION

Semiconductors and other electronic and opto-electronic assemblies are fabricated in groups on a wafer. Known as "dies", the individual devices are cut from the wafer and are then bonded to a carrier. The dies must be mechanically mounted and electrically connected to a circuit.

The above-incorporated parent applications describe a variety of means for producing substrates having conductors embedded beneath the surface of the substrate. The techniques disclosed therein provide increased conductor density and decreased inter-conductor spacing via embedded circuit technologies.

In particular substrate and method embodiments described in the above-incorporated patent applications, a plating or paste screening process is used to provide conductive material within channels formed in a substrate. The metal is generally plated to completely fill the channels, which generally include channels forming lands for solder ball attach, passive component attach and/or semiconductor die attach. The metal is then planarized to

isolate the conductors by removing the conductive material that is above the substrate surface, forming a circuit pattern that is embedded beneath the surface of the substrate. An etching process that removes the conductive material above the surface of the substrate is one of the planarization process options disclosed in the above-incorporated parent applications.

However, when a plating process is used to deposit the conductive material in the channels and/or when an etching process is employed to planarize the conductive material, variations in width of conductors, and in particular the size of lands affects the plating and/or planarization process, as the rate of conductor deposit or removal is directly related to the size of a feature. With respect to interconnect lands, which are typically circular for a solder ball or flip-chip attach land and square or rectangular for a surface mount (SMT) component package attach land (such as lands for attaching SMT resistors, capacitors, diode and transistors), the relatively large size of the land leads to a "dimpling" effect, in which a higher etching current density around large features increases the rate of material removal. The result of the increased removal rate is a "dimple" in the centers of larger features, and in extreme cases, a loss of conductive material in the center of the feature. In the case of plating processes used to deposit the channel material, larger features lead to increased material

build-up that is uneven and can result in the inability of the planarization process to remove the excess deposits.

Any of the above dimpling effects are undesirable, as the attachment region provided by the land becomes non-planar, which can affect solderball height for solderball attach lands, and planarity of SMT mounting lands. Variations in solderball height and planarity of SMT mounting lands can cause missed or weak interconnects to the substrate, resulting in failure of a circuit module.

Further, subsequent to the etching process, a further plating process is typically employed to provide improved solderability and/or protection of lands from environmental conditions such as oxidation by depositing gold or gold-nickel plating on the lands. The larger area of conductive features on the substrate such as the lands described above, increases the amount of plating material, which raises the cost of the plating procedure.

Therefore, it would be desirable to provide substrates having improved land planarity and a method of manufacturing the substrate, that reduce or eliminate the dimpling effect. It would further be desirable to provide a lower cost substrate and method of manufacturing the substrate that reduces plating costs.

SUMMARY OF THE INVENTION

The above objectives of reducing or eliminating dimpling and reducing plating cost are provided in a substrate and method for manufacturing a substrate. The substrate incorporates land feature shapes that reduce the contiguous conductive area of the land, thus reducing non-uniformity in the plating current density used to deposit conductive material during a plate-up process and the etching current density used to remove conductive material from above the substrate in a subsequent planarization process. The land shapes further decrease the amount of plating material required in subsequent plating operations that add precious metals for solderability and environmental protection.

The land shapes include sub-features such as interconnected lines or other interconnected geometric shapes that provide full land functionality, while reducing the area of the feature. The sub-features employed may be designed so that the line width of each sub-feature is the same as the line width of conductive patterns on the substrate, so that the etching process can be made completely or nearly completely uniform. A grid pattern may be employed, so that all of the sub-features intersect (providing electrical interconnection) while maintaining a uniform line width. Alternatively, in particular for circular features such as solderball lands, the features may be rings or

ring segments interconnected by segments of conductor, or may be other geometric shapes interconnected by segments of conductor, so that a larger attach area is provided, while reducing plating/etching current density for the land, eliminating or reducing the dimpling effect. The above-described features may also be employed to reduce the cost of subsequent plating operations such as gold or gold-nickel plating, as less material must be deposited on the lands of the present invention than on typical solid lands, thus reducing the plating cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1C are pictorial diagrams depicting a cross-sectional view of stages of preparation of an integrated circuit substrate in accordance with an embodiment of the present invention;

Figure 2A is a pictorial diagram depicting the cross-section of a land in accordance with an embodiment of the present invention;

Figures 2B and 2C are pictorial diagrams depicting cross-sections of lands exhibiting dimpling;

Figures 3A and 3B are pictorial diagrams depicting a top view and a cross-sectional view, respectively, of a land in accordance with an embodiment of the present invention;

Figure 3C is a top view of a land in accordance with another embodiment of the present invention;

Figures 4A-4C are pictorial diagrams depicting a top view of lands in accordance with other embodiments of the present invention; and

Figures 5A and 5B are pictorial diagrams depicting integrated circuits in accordance with embodiments of the present invention.

The invention, as well as a preferred mode of use and advantages thereof, will best be understood by reference to the following detailed description of illustrative embodiments when read in conjunction with the accompanying drawings, wherein like reference numerals indicate like parts throughout.

DETAILED DESCRIPTION

Referring now to the figures and in particular to Figure 1A-1C, a cross-sectional view of stages of preparation of a substrate in accordance with an embodiment of the present invention is shown. A first substrate stage 10A, having a dielectric top layer 12A, a dielectric bottom layer 12B and an optional core 11, which may be a metal ground plane layer or an insulating core, is prepared in accordance with techniques disclosed in the above-incorporated patent applications. Core 11 may be absent, in which case a single dielectric layer may be

prepared on one or both sides in accordance with techniques disclosed in the above-incorporated patent applications.

Substrate stage 10A includes laser-cut or imprinted channels and other features including circuit pattern channels 14A, blind vias 16A, through vias 16B, and features for providing various lands 18A-18C. The present invention concerns the formation and shapes of land features 18A-18C so that dimpling is prevented or reduced during a plating process and/or a subsequent planarization etching process, while providing an attachment area adequate for attachment of passive components, solderballs, integrated circuit die terminals and wire bonds. Plating material requirements are also reduced during subsequent precious metals plating processes that provide solderable lands and/or environmental protection.

The above-incorporated patent applications describe laser-ablation and/or imprinting techniques for forming channels and other features in dielectric layers 12A and 12B and also describe the subsequent preparation stages of substrate 10A as depicted in Figures 1B-1C herein.

Figure 1B depicts a substrate stage 10B in which metal layers 20A and 20B have been added to substrate stage 10A. The metal layers fill the conductive channels and other features so that conductive features may be provided for forming electrical connections between devices that are subsequently mounted on a

finished substrate to form an integrated circuit. Metal layers 20A and 20B may be plated, paste-screened or applied using other techniques as described in the above-incorporated patent applications. If metal layers 20A and 20B are plated, the lands of the present invention prevent an uneven deposit of plated-up material.

After metal layers 20A and 20B have been applied, a etching process may be employed to remove the excess metal above the surfaces of dielectric layers 12A and 12B, so that a conductive pattern including lands in accordance with embodiments of the present invention are provided on a completed substrate 10C as depicted in Figure 1C. After removal of the excess metal, further preparation processes may be applied to substrate 10C such as gold or nickel-gold plating of lands and application of solder masks. As the conductive channels within the substrates of the present invention may be produced by several combinations of techniques, it should be noticed that as long as one of the processes for depositing or planarizing the metal conductors involves etching or plating, the lands of the present invention will reduce or eliminate the dimpling effect and/or over-depositing of material. For example, the conductive material may be plated, but planarized using mechanical milling techniques, and the lands of the present invention will avoid the over-depositing of material in the larger land areas. Similarly, the

conductive material may be paste-screened to deposit the conductive material and then etched to planarize the material, in which case the lands of the present invention will avoid over-etching the larger land areas. Finally, for substrates that are plated and then etched, the lands of the present invention avoid both plating and etching non-uniformity.

While the description above and Figures 1A-1C describe stages of one or more processes formerly disclosed in the above-incorporated patent applications, it should be noted that substrate 1C and the prior preparation stages include feature shapes that reduce or eliminate dimpling in lands formed in substrate 1C and also reduce the amount of plating material required to plate the lands if a gold or nickel-gold plating process is employed in the final stages of substrate 10C preparation. Land shapes in accordance with embodiments of the present invention will be described in detail below.

Figures 2A-2C depict cross-sections of lands that exhibit various degrees of "dimpling". Figure 2A shows a desirable land 28B in accordance with an embodiment of the present invention, that has a surface 28B that is substantially planar and exhibits no "dimpling". Figure 2B shows a land with some dimpling effect, wherein surface 28B1 of the land has a concavity 29A produced by over-etching in the central area of the land. The over-etching is caused by increased current density in the electrochemical

etching process. The increase is exhibited in the central regions of large conductive areas such as lands. Concavity 29A will not generally prevent contact between a component terminal and the conductive material forming the land, but a gap is provided that may weaken the mechanical strength of an attachment made to the land.

Figure 2C depicts a land that is over-etched to form a concavity 29B that extends completely across the surface 28B2 of the land. Concavity 29B may cause a connection to be completely missed between a component terminal and the land. For example, in a flip-chip mounting configuration, if the land is a die terminal land, the terminal may not contact the land at all. If the land is a solderball land for providing external terminals in a ball grid array (BGA) package, a solderball may be attached to the land, but concavity 29B will cause a solderball height variation that will cause a failure in mounting the BGA package to an external mounting structure. Even moderate dimpling such as concavity 29A depicted in Figure 2B will cause variation in solderball height due to the extra solder required to fill concavity 29A.

Referring now to Figure 3A, a land 28B shaped in accordance with an embodiment of the present invention is depicted. Land 28B is a rectangular land provided for connection of surface mount (SMT) components and is formed in a grid pattern of

channels forming conductive lines 32 when filled with conductor and the conductor is planarized. Due to the uniform width of lines 32, the etching current density is made uniform and generally the width of lines 32 will be chosen to match the width of other channels within the substrate. Connection to land 28B may be provided by a circuit pattern 36 line, by a via connection 34 which may be a blind or through via, or by both types of connection. Figure 3B illustrates a cross-section showing the relationship of the grid lines 32 within dielectric layer 12A. The conductive lines 32 crossing from left to right in Figure 3A are shown by the dashed lines, so that the location of conductive lines 32 depicted vertically in Figure 3A can be shown within dielectric layer 12A. Land 28B provides sufficient contact area for solder attach of SMT components, while providing good planarity of the conductive line 32 surfaces forming land 28B, due to the elimination of the "dimpling" effect. Material applied to land 28B, such as gold or nickel-gold plating will be reduced according to the area reduction of the grid as opposed to a solid rectangular region, resulting in a lower final plating cost.

Figure 3C depicts a circular land 28A for solderball mounting, that is also formed in a grid pattern similar to that of rectangular land 28B. Interconnection can be provided by a via 34A, a conductive pattern 36A, or both as described above

for land 28B, and land 28A provides similar elimination of dimpling and plating costs as for grid 28B.

Referring now to Figures 4A-4C, alternative land designs for circular lands are depicted, such as lands suitable for solderball attach. Land 28A1 is a circular land formed from multiple circular regions 33A disposed radially about a larger central circular region 33B. The regions are connected by conductive channels 32B so that all of the regions are electrically connected. Land 28A1 provides a reduction in dimpling due to a current density reduction, while maintaining a larger central area than grid 28A of Figure 3A, which provides a greater mechanical attachment strength and may be preferable for external solderball terminal attachment points. Similarly, Land 28A2 is a circular land formed from multiple annular segments 33D disposed circumferentially at a common radius about a larger central circular region 33C. The regions are connected by conductive channels 32C so that all of the regions are electrically connected. Land 28A2 is an alternative to land 28A1 having similar properties of dimpling reduction while retaining a larger central area. Finally, Figure 4C depicts another circular land 28A3 that includes a circular central area 33E and a single annulus 33F disposed around central area 33E and connected by conductive channels 32D. Land 28A3 is another

alternative to land 28A1 having similar properties of dimpling reduction while retaining a larger central area.

Referring now to Figure 5A, an integrated circuit 50A, in accordance with an embodiment of the invention is shown. A die 52A is mounted on substrate 10C via a plurality of solder balls or posts 54 in a flip-chip configuration. A SMT component 53 is attached to lands 28B having a grid pattern as described above and as shown in a top view of the circuit area in balloon 55. External terminal solder balls 56 are added to the external terminal locations forming a complete integrated circuit package that may be subsequently encapsulated.

Referring now to Figure 5B, another integrated circuit 50B is shown exemplifying a wire bonded configuration. Die 26B is mounted to substrate 10C with an adhesive (generally epoxy) and wires 58 are bonded between plated lands formed in substrate 10D. A SMT component 53 is attached to lands 28B having a grid pattern as described above and as shown in a top view of the circuit area in balloon 55. Solder balls 56 are added to the external terminal locations. Substrate 10D is manufactured according to the same steps as substrate 10C, but has different circuit patterns, lands and die mounting area for accommodating wire-attach type die 52B.

The above description of embodiments of the invention is intended to be illustrative and not limiting. Other embodiments of this invention will be obvious to those skilled in the art in view of the above disclosure and fall within the scope of the present invention.